AND8346/D

A519HRT HART® Modem

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APPLICATION NOTE

Introduction

This application note describes a demonstration circuit that permits a user to implement a HART slave or master interface between a microprocessor and a process loop using the ON Semiconductor A5191HRT HART modem integrated circuit. The information in this application note is correct to the best of our knowledge. Development of a circuit suitable to the user's particular system and application environment is the responsibility of the user.

The HART (highway addressable remote transducer) communication protocol provides digital communication for microprocessor−based process control instruments. HART uses the Bell−202 forward channel signaling frequencies and bit rate (1200 bits/second) as making it a subset of the Bell−202 standard. HART−speaking devices can use virtually any Bell−202 standard modem. However, the ON Semiconductor A5191HRT single−chip modem has been designed to meet the low power requirements of 2−wire process instruments.

Features of the A5191HRT

- Same modem design as LSI 20C15
- Transmits a trapezoidal signal
- Internal oscillator cell
- Internal receive filter
- Carrier detect
- 28 pin PLCC package (green, RoHS compliant)
- 32 pin LQFP package (green, RoHS compliant)

The ON Semiconductor A5191HRT modem is designed to allow the user to easily implement a HART compliant physical layer design (HART FSK Physical Layer Specification; HCF_SPEC−54, Revision 8.1 November 24, 1999). The A5191HRT is intended to replace the LSI/NCR 20C15 for all existing and future HART applications. The A5191HRT is a near pin−for−pin replacement for the 20C15. The A5191HRT can be used in any circuit that uses the LSI 20C15 with no circuit topology changes. Only the values of four external resistors in the receive filter need to be changed.

This application note explains how to interface the A5191HRT modem to the HART network, as well as other general advice on using the modem and on designing HART devices. A block diagram showing a typical application of the A5191HRT in a HART Slave is shown in Figure 1.

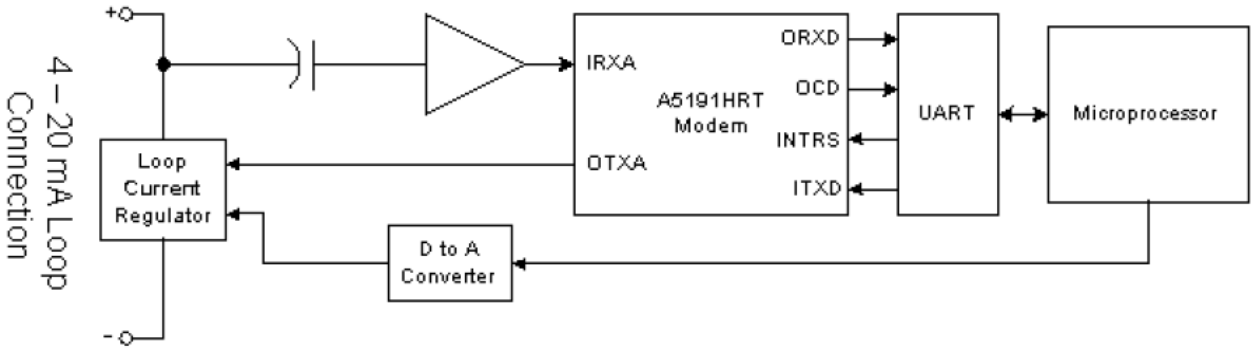

Figure 1. A5191HRT HART Slave Application Block Diagram

Overview of HART Communications

Analog Signaling

HART devices are connected in a current loop arrangement shown in Figure 2. The process transmitter (field instrument in HART specifications) signals by varying the amount of current flowing through itself. The controller (primary master) detects this current variation by measuring the DC voltage across the current sense resistor. The loop current varies from 4 to 20 mA at frequencies usually under 10 Hz.

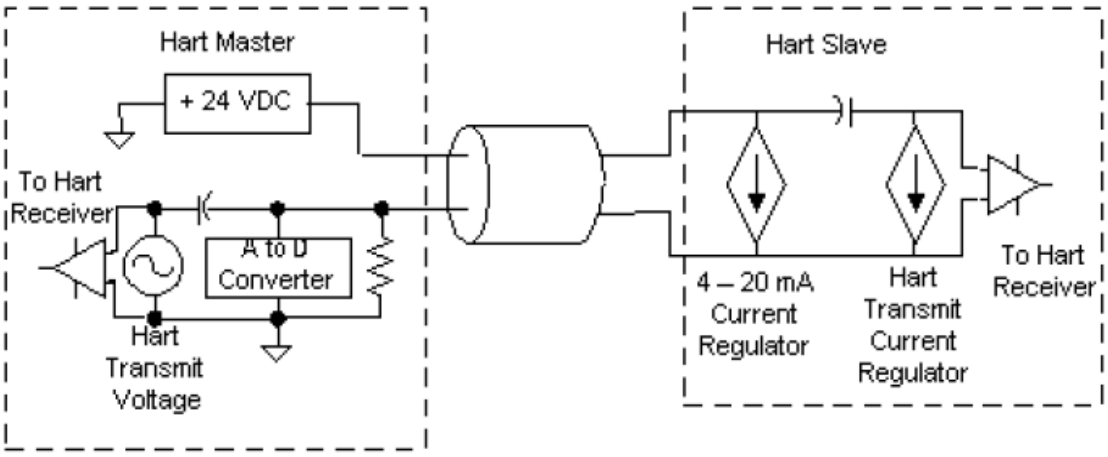

Figure 2. Conventional Current Loop with HART Signal Sources

Digital Signaling

The HART (digital) signal is superimposed on the 4−20 mA (analog) signal as shown in Figure 3. The master transmits HART signals by applying a voltage signal across the current sense resistor and it receives a voltage signal by detecting the HART current signal across the sense resistor. Conversely, the slave transmits by modulating the loop current with HART signals and receives HART signals by demodulating the loop current.

HART Waveform

HART signals using phase−continuous frequency−shift−keying (FSK) at 1200 bits/second. Phase−continuous FSK requires the phase angle of the mark (1200 Hz) and the space (2200 Hz) to remain continuous at the 1200 Hz bit boundaries. A field instrument transmits a HART signal by modulating a high−frequency carrier current of about 1 mAp−p onto its normal output current. This is illustrated in Figure 3 for a 6 mA analog signal.

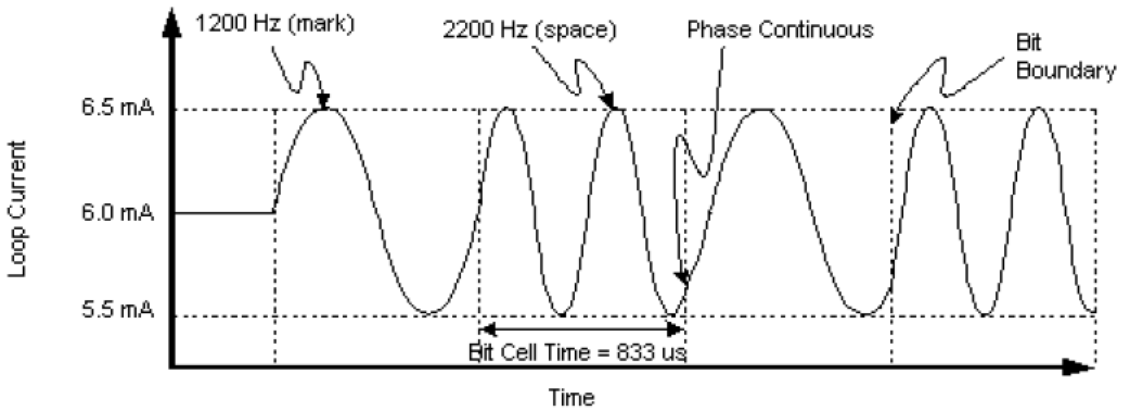

Figure 3. Field Instrument Current vs. Time

HART Slave Device

HART slaves transmit by modulating the process 4−20 mA DC loop current with a 1 mAp−p AC current signal as shown in Figure 3. Since the average value of the HART signal is zero, the DC value of the process loop remains unchanged. Receive circuits in a HART slave device amplify, filter and demodulate the current signal.

HART Multi−dropped Slave Devices

Some current loops (called networks in HART documents) use only digital signaling. The field instrument current is fixed at 4 mA or some other convenient value, and only digital communication occurs. Up to 15 such field instruments with unique addresses of 1 through 15 may be connected in parallel. A device that is not multi−dropped will usually have its address set to 0.

HART Master Device

HART masters transmit by driving the loop with a low impedance voltage source as shown in Figure 2. Regardless of whether a master or field device is transmitting, a signal voltage of about 500 mVp−p is developed across the conductors of the current loop (assuming a 500 Ω current sense resistor), and is seen by both devices. Receive circuits in each device filter and demodulate the signal voltage.

HART Primary Master

In general, a HART primary master is the device that provides the communications between the control system (DCS) and the remote process instruments with the intent to receive process information and perform maintenance operations. A HART network that has a HART master interface integrated into the DCS will usually be configured as a primary master.

HART Secondary Master

In general, a second HART interface connected to a network that contains a master will be a secondary master. An example of a secondary master is a hand−held communicator that would be connected directly across a HART. Such a network may have a primary master. A HART network can only have one primary and one secondary master connected at a time.

Multiplexing a HART Master

To reduce the design complexity of a multiple loop HART master, the physical layer can be multiplexed to two or more process loops. This is usually done with analog switches that allow signals as high as 16 Vp−p to pass and exhibit an extremely low on resistance. The added impedance of the switch directly affects the output impedance of the master device.

The multiplexer can switch only the HART signal or it can switch both the HART signal and the associated signal return. Switching the signal return insures the physical layer interface will be non−intrusive to the HART network if a failure were to occur. Typically, the analog switches connect to each process loop through a coupling capacitor (about 2.2 μF).

The greatest disadvantage of multiplexing HART signals is the reduction in communication throughput to each slave device.

HART Cabling

Because of the relatively low HART frequencies there is little cable attenuation and delay distortion. This results in very few restrictions on constructing networks. The complete topology requirements and electrical requirements for HART devices are given in the HART physical layer specification (2).

In most applications, HART communications can be performed up to a distance of 5000 feet (1500 meters) using existing field wiring for a 2−wire process instrument.

HART Data Link Layer

Normally, one HART device talks while others listen. Talking means applying the modulated carrier to the network cable. A given device applies carrier in one unbroken segment called a frame. Between frames the network is silent. Field instrument frames are usually responses to commands by a master. Further information on network protocol is found in the HART data link layer specification (1).

Signal Description

Table 1. 28 Pin PLCC Pin Descriptions

Pin No.	Symbol	Pin Name	I/O
1	TEST1	Connect to VSS	
2	TEST2	No connect	
3	TEST3	No connect	
4	TEST4	No connect	
5	TEST5	Connect to VSS	
6	INRESET	Reset all digital logic when low, normal operation when high. This pin is intended to be used as a power−on−reset (POR). See the HART Slave section of this application note and section 3, Figure 3 of the data sheet for detailed information on the requirements for POR operation.	
7	TEST7	Connect to VSS	
8	TEST8	Connect to VSS	
9	TEST9	Connect to VSS	
10	OTXA	Transmit analog output. OTXA is a trapezoidal signal controlled by ITXD. ITXD = logic low = 2200 Hz. ITXD = logic high = 1200 Hz. Active when INRTS is low, 0.5 VDC when INRTS is high.	O
11	IAREF	Analog reference input 1.2 to 2.6 VDC, typically 1.23 VDC	I
12	ICDREF	Carrier detect reference voltage input, typically 1.15 VDC (IAREF − 0.08 VDC)	I
13	OCBIAS	Bias current set. External resistor sets the bias current. IAREF/Rbias = 2.5 mA ±5%	O
14	TEST10	Connect to VSS	
15	VDDA	Analog VDD	I
16	IRXA	Receive analog input. Accepts 1200/2200 Hz signals from the external filter.	I
17	ORXAF	The square wave output of the high pass filter	O
18	IRXAC	The positive input of the carrier detect comparator and receiver filter comparator	I
19	OXTL	Oscillator output: 460.8 kHz	O
20	IXTL	Oscillator input: 460.8 kHz	I
21	VSS	Analog/digital ground	I
22	VDD	Digital VDD	I
23	INRTS	Request to send input. Selects operation of the modulator. When low asserts OTXA. When high sets OTXA = 0.5 V. Must be high during power−up.	I
24	ITXD	Transmit digital input. Logic high = mark (1200 Hz), logic low = space (2200 Hz)	I
25	TEST11	No connect	
26	ORXD	Receive digital output. Logic high = mark (1200 Hz), logic low = space (2200 Hz). ORXD is qualified with OCD.	O
27	OCD	Carrier detect output. It goes high if the received signal is larger than the ICDREF for 4 cycles of IRXA signal.	O
28	TEST12	No connect	

32 Pin LQFP

Table 2. 32 Pin LQFP Pin Descriptions

Pin No.	Symbol	Pin Name
1	TEST5	Connect to VSS
2	INRESET	Reset all digital logic when low, normal operation when high. This pin is intended to be used as a power−on−reset (POR). See the HART Slave section of this application note and section 3, Figure 3 of the data sheet for detailed information on the requirements for POR operation.
3	TEST7	Connect to VSS
4	TEST8	Connect to VSS
5	TEST9	Connect to VSS
6	VSS	Digital ground*
7	OTXA	Output transmit analog. FSK modulated HART transmit signal to 4 to 20 mA loop interface circuit.
8	IAREF	Analog reference voltage
9	ICDREF	Carrier detect reference voltage
10	OCBIAS	Comparator bias current
11	TEST10	Connect to VSS
12	VSSA	Analog ground*
13	VDDA	Analog supply voltage
14	IRXA	FSK modulated HART receive signal from 4−20 mA loop interface circuit
15	ORXAF	Analog receive filter output
16	IRXAC	Analog receive comparator input
17	OXTL	Crystal oscillator output
18	IXTL	Crystal oscillator input
19	VSSA	Analog ground*
20	VSS	Digital ground*
21	VDD	Digital supply voltage
22	INRTS	Request to send
23	ITXD	Input transmit data. Transmitted HART data stream from UART.
24	TEST11	No connect
25	ORXD	Received demodulated HART data to UART
26	OCD	Carrier detect output
27	TEST12	No connect
28	TEST1	Connect to VSS
29	TEST2	No connect
30	VDD	Digital supply voltage
31	TEST3	No connect
32	TEST4	No connect

*On the 32 LQFP the analog ground and digital ground pins must be connected together externally and connected to the system power ground. The separate 32 LQFP grounds help decrease the ground noise coupled into the chip. On the 28 PLCC version there are not separate analog and digital grounds. In the 28 PLCC these two grounds are connected inside the package to minimize pin count.

A5191HRT Functional Blocks

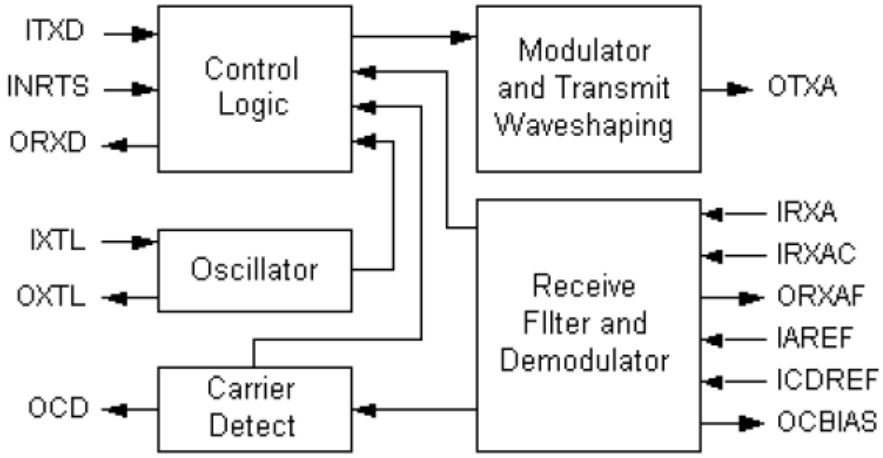

Figure 4. A5191HRT Block Diagram

HART Modem

Demodulator

The demodulator accepts an FSK signal at its IRXA input and reproduces the original modulating signal at its ORXD output shown in Figure 5.

The modem uses shift frequencies of nominally 1200 Hz (logical one, mark) and 2200 Hz (logical zero, space). The bit rate is nominally 1200 bits/second. The output of the modulator ORXD is qualified with the carrier detect signal OCD. Therefore only IRXA signals large enough to be detected (100 mVp−p typical) by the carrier detect function will produce demodulated output at ORXD.

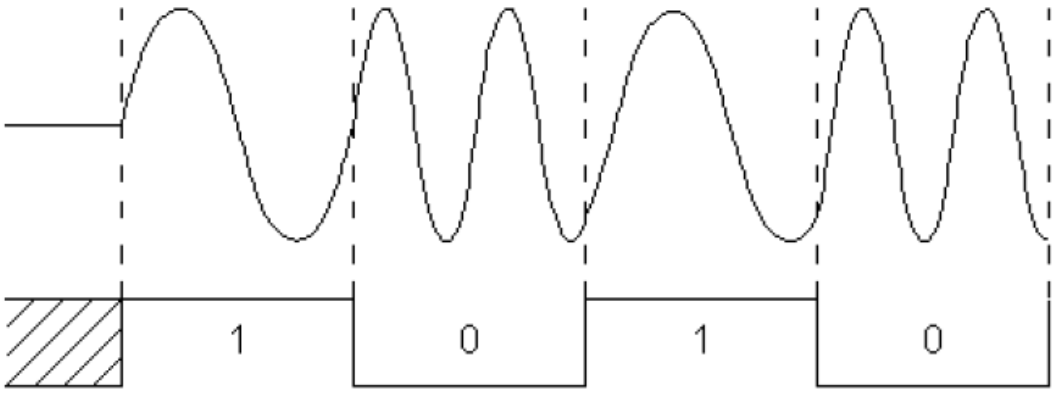

Figure 5. Demodulator Signal Timing

Modulator

The modulator accepts digital data in NRZ form at its ITXD input and generates the FSK modulated signal at its OTXA output. INRTS must be a logic low for the modulator to be active.

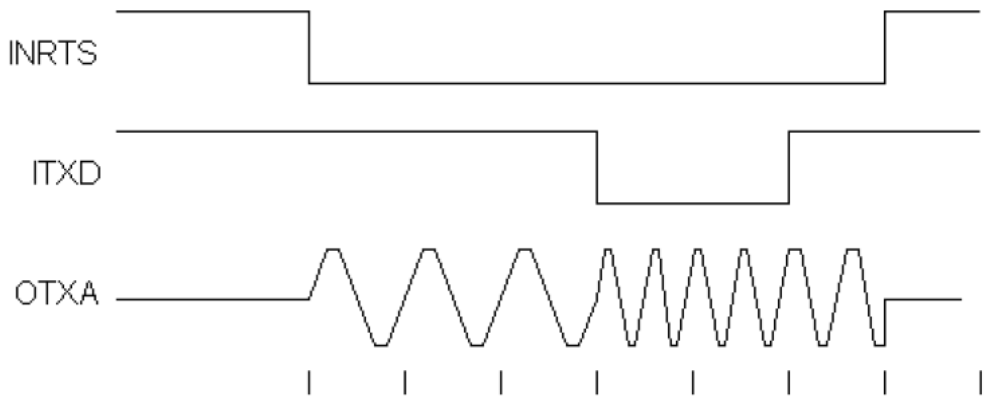

Figure 6. Modulator Signal Timing

Transmit Waveshaping

The A5191HRT generates a HART compliant trapezoidal FSK modulated signal at its OTXA output. Shown below are actual transmit signals from a A5191HRT.

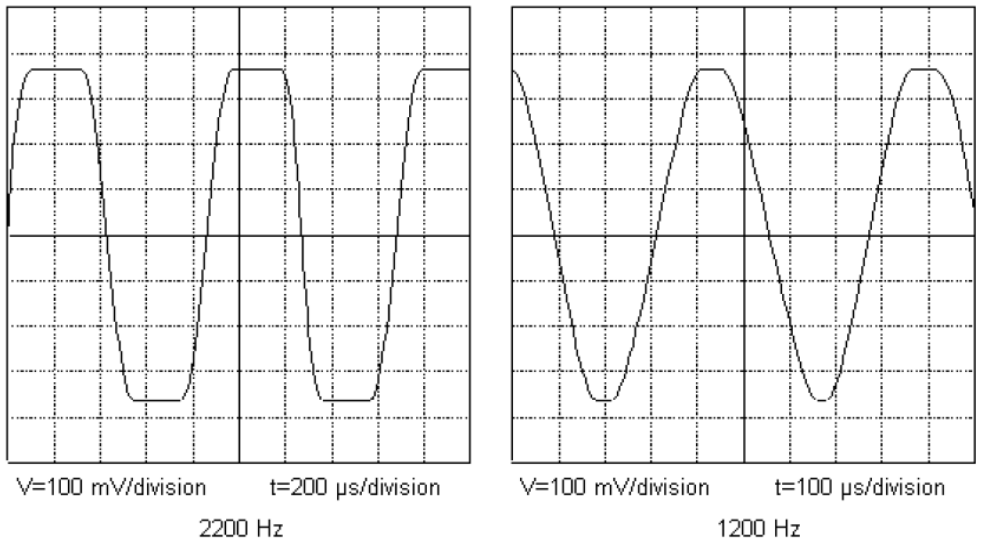

Figure 7. OTXA Waveform

The amplitude of OTXA is proportional to the analog reference voltage as follows:

OTXAp−p = IAREF x 0.417
For IAREF = 1.235 VDC
OTXAp−p = 1.235 x 0.417 = 0.515 Vp−p
A voltage swing from 0.16 to 0.77 VDC
When IRTS = logic high; OTXA = 0.5 VDC
(When AREF = 1.235 VDC)

Carrier Detect

The A5191HRT implements a carrier detect (CD) that is compliant with the HART physical layer specification which requires the receiver to activate CD between the incoming signal levels of 80 and 120 mVp−p. Carrier detect will be compliant when ICDREF − IAREF = 0.08 VDC. The circuit shown in the appendix is designed for a nominal CD level of 100 mVp−p.

Internal to the A5191HRT, a comparator asserts a logic low if the IRXAC voltage is below ICDREF. The comparator output is fed into the carrier detect block, which asserts the output pin OCD to a logic high if INRTS is a logic high, and four consecutive pulses out of the comparator have arrived. The carrier detect output OCD stays at a logic high as long as INRTS is at a logic high and the next comparator

pulse is received in less than 2.5 ms. Once OCD goes inactive to a logic low, it takes four consecutive pulses out of the comparator to set OCD to a logic high again. Four consecutive pulses amount to 3.33 ms when the received signal is 1200 Hz and to 1.82 ms when the received signal is 2200 Hz.

Clock Oscillator

The A5191HRT requires an external 460.8 kHz clock, ceramic resonator, or crystal, accurate to at least 1%. The oscillator requires two external capacitors and one external resistor, which varies depending on the type of the crystal/resonator. The specifications are listed in the two tables below. The A5191HRT has an internal oscillator cell, only requiring an external ceramic resonator and two capacitors. The oscillator cell is designed to use either a crystal, ceramic resonator or an external clock. When using a ceramic resonator or crystal, care should be taken to keep the circuit board traces between the A5191HRT and the external oscillator components as short as possible.

Ceramic Resonator Sources

Ceramic resonators are less expensive than crystals, but are not as accurate. Unfortunately, ceramic resonators at the needed frequency require special ordering in very large quantities. Ceramic resonators that oscillate at 460 kHz are available from:

MuRata Erie North America, Inc.
2200 Lake Park Drive
Smyrna, GA 30080
Tel: 770−436−1300

Raltron Electronics Corp.
10651 Northwest 19th St.
Miami, Florida 33172
Tel: 305−593−6033, Fax: 305−593−3973

External Clock

It may be desirable to use an external clock (460.8 kHz) rather than the internal oscillator cell because of the cost and availability of ceramic resonators. In addition, the A5191HRT consumes less current when an external clock is used as shown below in Figure 8. An external clock associated with the microprocessor (running at a frequency that is a multiple of 460.8 kHz) can be used as an input to the oscillator cell. The interface between the microprocessor clock and the A5191HRT could be as simple as a direct connection or a single integrated circuit.

Note: output OXTL is driven by an external source.

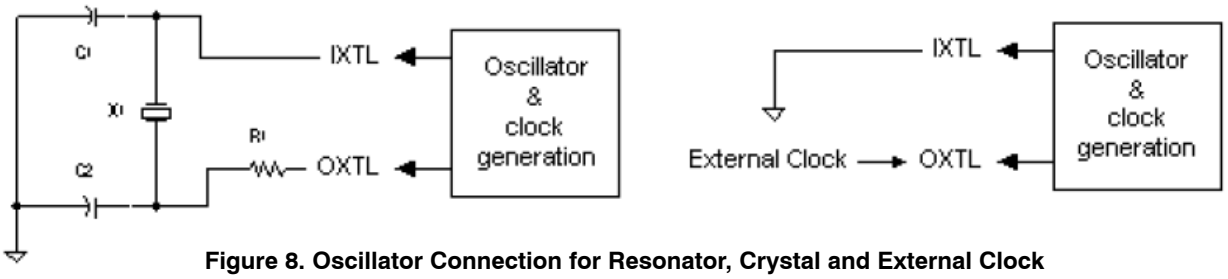

Figure 8. Oscillator Connection for Resonator, Crystal and External Clock

Table 3. Resonator and Crystal Values

Description	Suggestion #1	Suggestion #2
Crystal Frequency	460.8 kHz	460.8 kHz
C1	220 pF	47 pF
C2	220 pF	22 pF
R1	<500 Ω	10 kΩ
Vendor / Xtal−type	Ceramic Murata−Erie CSB series	Quartz Statek CX−1V
XTAL ESR (Max)	−	12 kΩ

Clock Skew

If you use the same time base for both the modem and the UART, a 1% accurate time base may not be good enough. The problem is a combination of receive data jitter and clock skew between transmitting and receiving HART devices. If the transmit time base is at 99% of nominal and the receive time base in another device is at 101% of nominal, the receive data (at the receiving UART) will be skewed by roughly 21% of one bit time at the end of each 11−bit byte. This is shown below in Figure 9. The skew time is measured from the initial falling edge of the start bit to the center of the 11th bit cell.

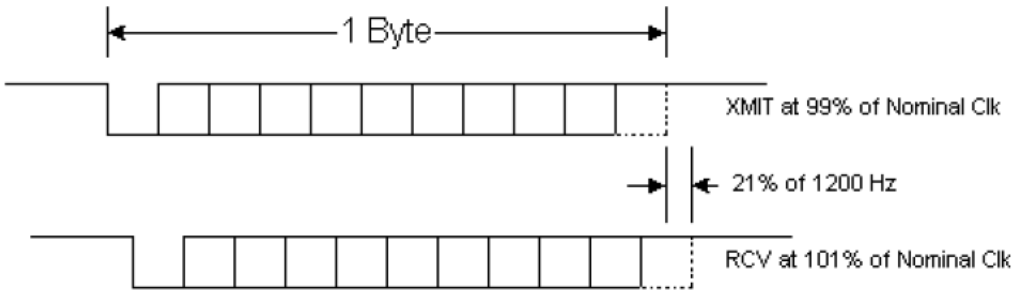

Figure 9. Clock Skew

This 21% skew by itself isn't bad. However, there is another error source for bit boundary jitter. The phase lock loop demodulator in the A5191HRT produces jitter in the receive data that can be as large as 12% of a bit time. Therefore, a bit boundary can be shifted by as much as 24% of a bit time relative to its ideal location based on the start−bit transition. (The start−bit transition and a later transition can be shifted in opposite directions for a total of 24%.)

The clock skew and jitter added together is 45%, which is the amount that a bit boundary could be shifted from its expected position. UARTs that sample at mid−bit will not be affected. However, there are UARTs that take multiple samples during each bit to try to improve on error performance. These UARTs may not be satisfactory, depending on how close the samples are to each other, and how samples are interpreted. A UART that takes a majority vote of three samples is acceptable.

Even if your own time base is perfect, you still must plan on a possible 35% shift in a bit boundary since you don't have control over time bases in other HART devices.

Receive Analog Circuitry

Receive High−pass Filter

To remove the interfering analog signal, a high−pass filter is required in the HART signal receive path. The filter requirements are found as follows. From section 7.1 of the HART physical layer specification, the interfering signal can be as high as 16 Vp−p at 25 Hz. *(NOTE: This is directly related to limits on analog signaling. The difference in specifications for analog interference as output versus analog interference as input is the result of the loads being different.)* The interfering analog signal should be reduced to at least ten times smaller than the smallest HART signal, or under about 7.5 mV. Therefore, the high−pass filter should have an attenuation of 63 dB at 25 Hz. The HART signal band covers approximately 950 Hz to 2500 Hz, which means that the high−pass filter should begin rolling off somewhere below 950 Hz and be 63 dB down at 25 Hz. This is illustrated in Figure 10.

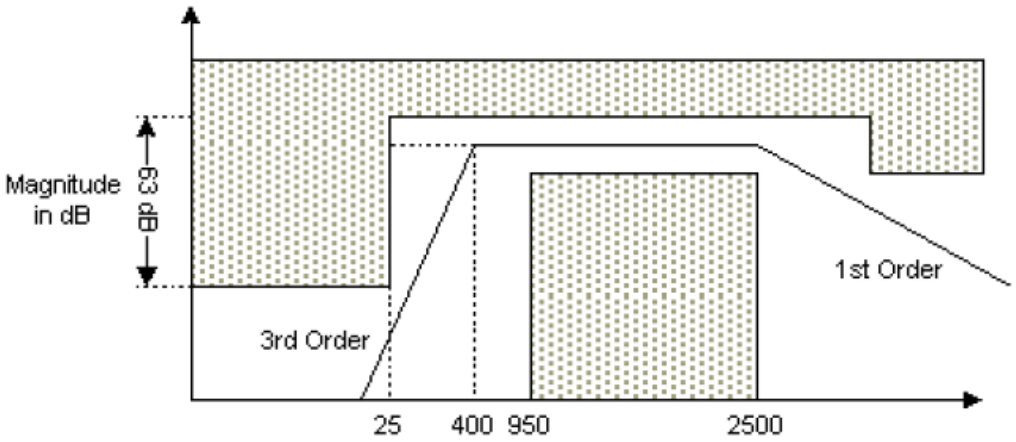

Figure 10. Receive Filter Bounds

The A5191HRT has an internal active filter to attenuate the frequencies outside the HART bandpass. In addition to the internal active filter, an external passive filter is necessary to complete the filtering requirements. The external capacitors and resistor were too large in size to cost effectively integrate into the A5191HRT silicon.

The external components required for the receive filter is shown in Figure 11. All the external capacitors are ±5% and the resistors are ±1% components (except the 3 MΩ is ±5%).

The external components on the receiver create a three pole high pass filter at 624 Hz and a one pole low pass filter at 2500 Hz. Internally, the A5191HRT has a high pass pole

at 35 Hz and a low pass pole at 90 kHz, each of which can vary by as much as ±30%. The input impedance to the entire filter is greater than 150 K at frequencies less than 50 kHz.

In Figure 11 there are four resistors circled. The value of these resistors is different than those used in the LSI 20C15. The four resistor values were changed because the A5191HRT is not exactly the same as the 20C15. They are both made using 0.5 μm CMOS processes and the general architectures of the two chips are identical. However, the receive filter amplifier and receive comparator (see Figure 8) in the A5191HRT are slightly different than in the 20C15. It is impossible to make an analog part identical in two different processes in two different fabrication facilities.

The biggest difference between the two parts and the major contributor to the need to change the four resistor values when using the A5191HRT are in the receive demodulator. This block is quite different in the A5191HRT. This section was changed because even though the 20C15 passed all the conformance tests, it barely passed. The different resistor values change the shape of the lower pass band for the receive filter. These changes provide more margin in passing the out−of−band noise interference tests. This in turn makes for a more robust and noise immune receiver.

Table 4. Resistor Value Changes Between the A5191HRT and 20C15

	ON Semiconductor A5191HRT	LSI20C15
R5	215 k	402 k
R4	215 k	453 k
R1	499 k	825 k
R6	422 k	732 k

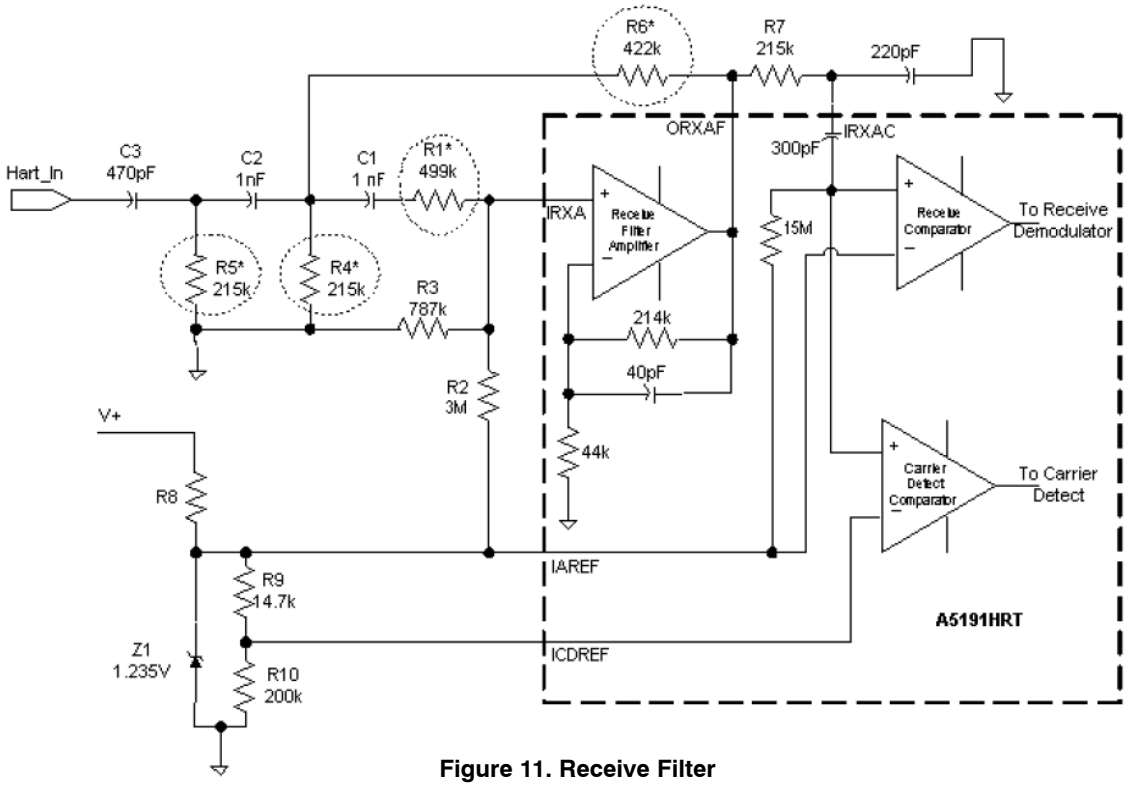

Figure 11. Receive Filter

The values shown in Figure 11 for R9 and R10 may be different than those used in some 20C15 applications. The ratio of these two resistors sets the receive threshold. In some 20C15 designs the value of R9 is 15 k and/or the value of R10 may be 215 k. The exact values may differ from design to design. The values shown for all external components in Figure 11 and all other circuits in this application note are those used in the circuitry which was used to pass the HART physical layer conformance test for the A5191HRT.

Voltage References

The A5191HRT requires two voltage references, IAREF and ICDREF.

IAREF sets the DC operating point of the internal op−amps and comparators and is usually selected to split the DC potential between VDD and VSS. The A5191HRT requires a voltage reference (low power if necessary) with an output voltage level between 1.2 and 2.6 VDC. In the case of a 5 VDC supply, IAREF is typically 2.5 VDC. When operating as low as 3.0 VDC, a 1.235 VDC reference (Analog Devices AD589) is suitable as IAREF.

The level at which CD (carrier detect) becomes active is determined by the DC voltage difference between ICDREF and IAREF. Selecting IAREF − ICDREF = 0.08 VDC will set the carrier detect to a nominal 100 mVp−p.

Analog Bias Resistor

The A5191HRT requires a bias current set resistor tied between OCBIAS and VSS. The bias current controls the operating parameters of the internal op−amps and comparators. The value of the bias current set resistor is determined by the reference voltage IAREF.

The recommended value of the bias current set resistor is 499 kΩ when IAREF = 1.235 VDC.

Rbias = IAREF/2.5 mA

Current Budget and Transmitter Lift−off Voltage

Current consumption of internal circuits is important in any two−wire field instrument. It becomes critically important in a microprocessor−based field instrument featuring both analog and digital signaling. The available current is derived here and some techniques are examined for reducing current consumption.

The nominal HART signal transmitted by a field instrument is 0.5 mA peak. When this is superimposed upon a 4 mA analog signal, the terminal current must vary between 3.5 mA and 4.5 mA. During the peak of the HART waveform, the instrument has 4.5 mA available, but during the valley it has only 3.5 mA. Energy storage techniques can be used to allow the internal circuits to draw a steady 4 mA at all times. However, to be effective at HART frequencies, the storage capacitor is quite large. A large capacitor (or any form of energy storage device) complicates the circuit design if intrinsic safety is required. Therefore, normally only 3.5 mA is used to run everything. Another 200 to 400 μA is often subtracted from this to allow some margin and to satisfy other conditions. Assuming that the value is 200 μA, during transmit the internal circuits of the two−wire field instrument have to live on a diet of 3.3 mA. During receive there is 3.8 mA available.

A characteristic of the A5191HRT is that its current consumption is approximately 350 to 450 μA. This leads to the fortunate circumstance that the remaining (non−modem) circuits always have at least 3.25 mA available. Margins may be needed to cover current consumption over temperature. One way of reducing the A5191HRT current consumption is to operate it at reduced voltage. Since the A5191HRT is a CMOS part, current consumption is roughly proportional to supply voltage. This is evident in the graph contained in the appendix. Operation at 3.5 V is common.

In applying the A5191HRT be careful not to let inputs float. The IRTS pin of the A5191HRT will often be driven by an I/O pin of a microprocessor. During power−up or after reset an I/O pin may be tristated, allowing it to float. This can cause the A5191HRT to draw excess current. In some cases the current may be large enough to prevent the field instrument from starting up properly. There should be a 1 MΩ pullup resistor on IRTS.

The transmitter lift−off voltage is the minimum terminal voltage at which it is guaranteed to operate. When only analog signaling is involved, liftoff voltage is an unambiguous quantity. But when HART digital signaling is added, the available voltage can swing by as much as 0.75 V above and below the DC level. The minimum applied voltage is the DC level minus 0.75 V. You should either design the field instrument to accommodate the dips in voltage, or else specify the lift−off voltage to include them.

Interfacing to the HART Network

The slave interface to the network is typically a current regulator, as illustrated in simplified form in Figure 12. Its output current is controlled by varying a much smaller current into an op−amp summing junction. This junction is a convenient point at which to sum the analog and digital signals, thereby achieving superposition of the digital signal onto the analog. The digital transmit signal (OTXA) is capacitively coupled into the summing junction to preserve DC accuracy of the 4−20 mA analog signal. Also shown in Figure 12 is the receive path, consisting of a capacitor from the collector of the current regulator transistor to a high−impedance amplifier. Both the receive amplifier and the transmit current source should present a high impedance (greater than 100 kΩ) to the network.

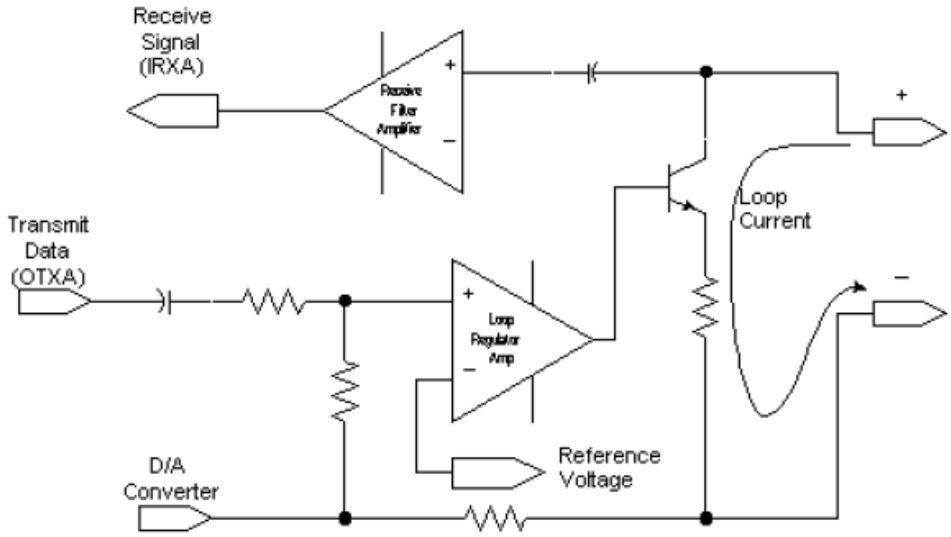

Figure 12. Simplified HART Slave Interface Circuit

Transmit Interface

The amplitude of OTXA is nominally 500 mVp−p. The HART physical layer requires the slave to modulate the loop with a 1 mAp−p signal. The amplitude of modulation of the loop current will have to be adjusted before the amplifier in the current loop regulator or at the regulator itself. It is recommended that the amplitude can be adjusted with voltage gain circuits. Using a small series capacitance to attenuate the signal may cause distortion of the transmitted signal.

Receive Interface

All HART receivers require non−disruptive coupling to the network current loop. This connection can be made with capacitive or inductive coupling without corruption of the process loop current. Typically a HART slave uses a small value (1000 pF) capacitor to couple an adequate signal level to the receive filter.

Master Device

The HART master interfaces to the network as a voltage source as illustrated in simplified form in Figure 13. The network is driven by a low output impedance (600 Ω or less) voltage amplifier circuit that can be switched to a high impedance state using INRTS. The output of the voltage amplifier needs to be a high impedance while the HART master receives, to insure a high input impedance for the receiver. Typically a HART master uses a 2.2 μF coupling capacitor to insure the transmitter circuit meets the output impedance requirements specified in the HART physical layer specification.

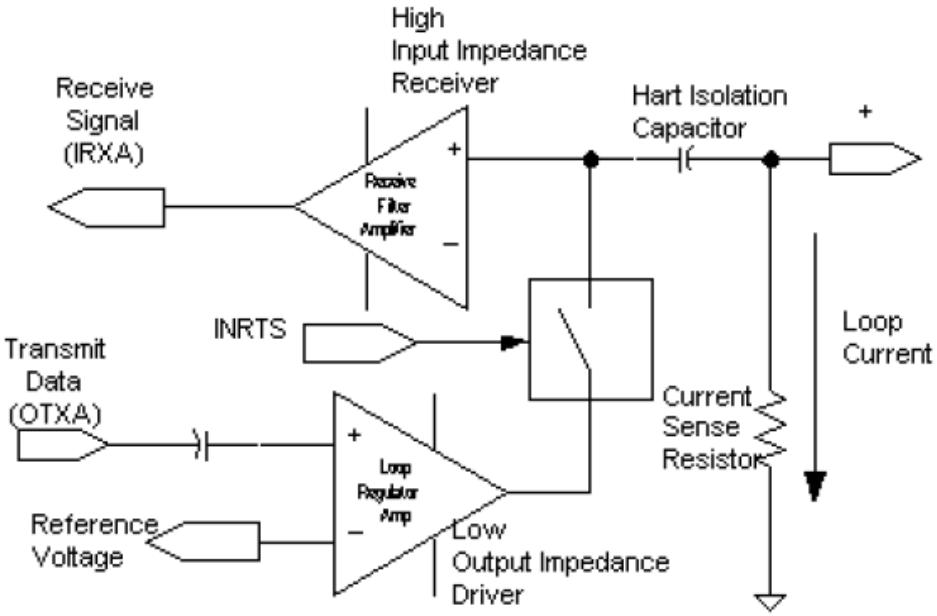

Figure 13. Simplified HART Master Interface Circuit

Transmit Interface

The amplitude of OTXA is nominally 500 mVp−p. The 500 mVp−p meets the requirements for a HART master. However, the A5191HRT is unable to source enough current to drive a HART network, therefore a low impedance voltage driver is required between the A5191HRT and the network.

Transmit Switch

During a HART message transmission from the master, the output impedance of the voltage source is quite low (0 – 600 Ω). However during reception of a HART message, the input impedance of the receive section must be quite high. Therefore, the transmitter section must be disabled when not active (INRTS “high”).

Several methods can be used to achieve a high output impedance of the transmitter while INRTS is inactive. One method is choosing an opamp with an active low current programming resistor that will basically turn−off the op−amp during receive operations. A second method can be implemented with a correctly biased discrete FET in series with the output stage. Lastly, a discrete solid−state relay with a characteristically low on resistance can be used.

All three techniques will provide an adequate solution for the impedance requirements. However, only the third solution will allow proper circuit operation per the bit−error−rate requirements and need not be powered by a dual supply. Under a worse case scenario, a transmitter could dynamically change from 4 – 20 mA and a HART master could have as much as 1000 Ω of loop resistance. This results in a 16 Vp−p low frequency carrier with HART superimposed. The transmit switch must be designed to prevent this 16 Vp−p signal from sinking current through the HART transmitter’s output stage. Any clipping of the 16 Vp−p signal through the HART transmitter or the use of transient suppressors will result in the clipping of the superimposed HART signal. The last solution will block and not clip the 16 Vp−p process signal and will not corrupt the input impedance. The third solution can be implemented easily as shown in Figure 21.

Receiving the HART Signal

HART Signal Coupling

All HART receivers require non−disruptive coupling to the network current loop. This connection can be made with capacitive or galvanic coupling without corruption of the process loop current. A receiver in a master may use a single 2.2 μF capacitor to couple the HART signal in which the master is always connected across a current sense resistor and share the same ground. Where ground isolation is required, another coupling capacitor may be necessary in the signal return connection.

To insure complete isolation from the network, galvanic isolation is the preferred method. Typically a transformer and a series capacitor are used to couple the HART signal. With this type of isolation, the master can be connected across the field instrument or the current sense resistor regardless of the polarity or grounding configuration.

Current Sense Resistor

The current sense resistor is considered an integral part of a HART master. In operation, a HART message response from a slave is superimposed on the 4 to 20 mA current loop. The slave’s 1 mAp−p HART signal is dropped across the master’s sense resistor. For a typical sense resistor of 250 Ω, one can expect 250 mVp−p signal extracted from a HART slave device. A HART master can have a sense resistor ranging from 230 Ω to 600 Ω.

Master Connection to a HART Network

A HART master must be able to receive voltage signals that are developed across the sense impedance. In addition, it must be able to apply a transmit signal across the current sense impedance. In some cases the master will signal across the field device as well. In all cases, the presence of the HART master must not disrupt the analog signaling of the process loop. Therefore, the HART signals must be non−intrusively coupled from the current sense resistor to the master through one of the various coupling techniques listed below. Coupling to the network is most commonly done with capacitors and transformers.

Basic Connection for DC Isolation

The simplest form of coupling is a single capacitor as shown in Figure 14.

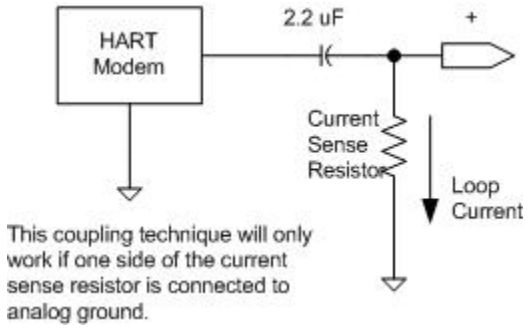

Figure 14. Single Capacitive Coupling

Floating Isolation Options

Using two capacitors will allow a connection across a sense resistor or field device that does not have one of its connections at analog ground as shown in Figure 15.

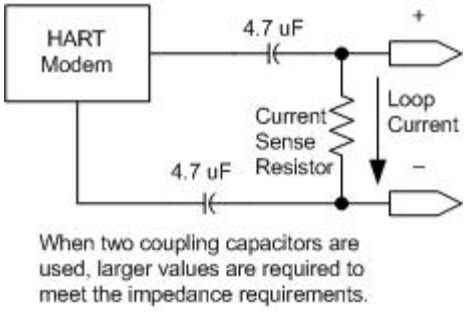

Figure 15. Dual Capacitive Coupling

Capacitive coupling can work well when masters have their power isolated from ground. When the system power configuration is unknown, the use of transformer coupling will insure the elimination of ground effects. An example of transformer coupling is shown in Figure 16.

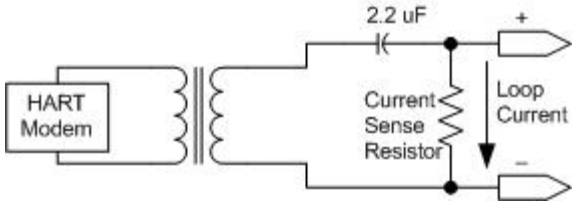

Figure 16. Transformer Coupling

Note on Grounding Effects

With the use of capacitive coupling, AC and DC ground loops can be created if one is not aware of the grounding techniques of both the master and the process loop. If the master is powered from a battery or a galvanically isolated power source, then single capacitive coupling will work in any HART network.

If a master (that does not have an isolated power source) with single capacitive coupling is connected to a sense resistor or field device that is not at ground potential, a DC ground loop will occur as shown in Figure 17.

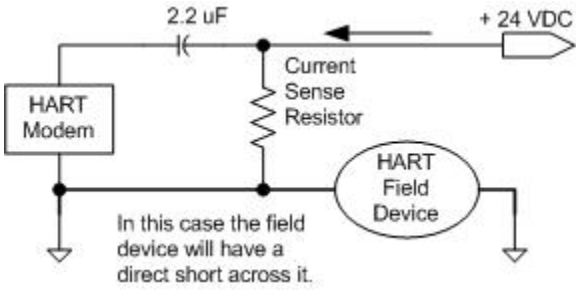

Figure 17. Single Capacitor Coupled DC Ground Loop

If the master has a ground connection that is not at the same ground potential as the analog ground from the process loop, it is possible to create AC ground loops. A noisy 110 VAC ground signal could be coupled directly into the process loop ground (single capacitive coupling) or coupled into the process loop (dual capacitive coupling) ground through the connection. The AC noise potentially could impede HART communications and corrupt the accuracy of the DCS measuring the analog current as shown in Figure 18.

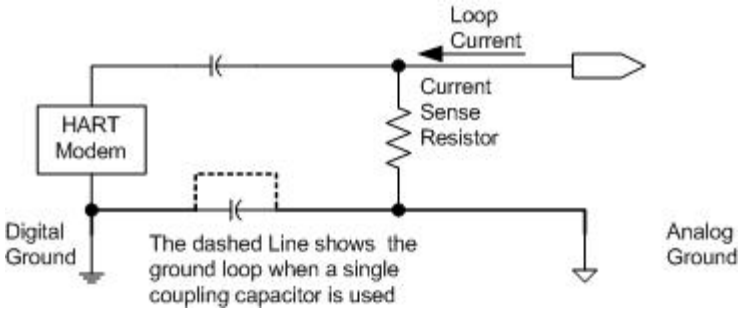

Figure 18. Capacitor Coupled AC Ground Loop

Band Limiting the Analog Signal

Band limiting the analog signal applies a HART slave and determines how fast it can control its output current. For a HART master the information in this section is provided to better understand the analog and digital signaling characteristics of a HART master.

Digital signaling can potentially interfere with analog signaling. A much worse problem is the analog signal interfering with digital signaling. This is due to the relative size of the two signals. For example, a change from 4 to 20 mA can produce a voltage change of as high as 16 V across the field instrument terminals, depending on the amount of resistance in the loop. At the same time, the instrument may be trying to detect a HART (digital) signal as low as 80 mVp−p.

Separating the two is usually done with a combination of low−pass filtering of the analog signal and high−pass filtering of the HART signal. The HART physical layer

specification (section 7.2) limits the analog signal to 16 mAp−p at frequencies below 25 Hz and constrains the output above 25 Hz to fall within a −40 dB/decade slope, as illustrated in Figure 19. This means, for example, that a sinusoidal output at 25 Hz must have an amplitude (into the 500 Ω test load) of less than 8 Vp−p. It also means that a 25 Hz square wave of 8 Vp−p would not be acceptable, since its harmonics do not decrease at a −40 dB rate.

The required roll−off of the analog signal can be achieved by various means, including:

1. Analog filters
2. Digital filters (software)
3. Inherent filtering in the instrument sensor

Often it is a combination of these. Any convenient method may be used to insure that changes in instrument output current fall within the specification. If the field instrument uses a D/A converter (DAC) to generate its analog output, the output steps of the DAC must be sufficiently small or else the high−frequency content of the steps must be removed by filtering. When large changes in the DAC output occur due to calibration operations, caution must be used not to have these DAC changes active during a HART command or response. Any large and fast current changes that fall outside the HART specifications can cause unreliable communications with the HART master or slave.

The analog signaling of typical field instruments is usually band−limited to the range of 1 to 10 Hz so that the roll−off starts well below the 25 Hz point of Figure 19. This can lead to simpler low− pass filtering. For example, a single−pole filter that begins rolling off at 1 Hz falls below the curve of Figure 19.

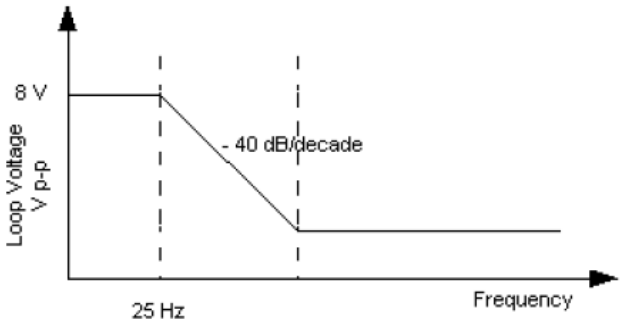

Figure 19. Amplitude Limit Versus Frequency

Miscellaneous

Start of Frame

Because the HART carrier must be started and stopped, the receiving UART and processor must become synchronized to each HART frame. During the synchronization period at the beginning of the frame, it is normal for some transmitted bytes to be corrupted or lost. Various HART requirements have been devised to insure that synchronization will occur. They are:

- The transmitting device must send at least five preamble bytes (hex FF).
- The transmitting device must load the first preamble byte into the transmit UART within five bit times of starting carrier.
- The receiving device must recognize carrier within 30 bit times.

Correct start−up is based on the fact that, during the stream of preamble bytes, the start bits (applied to the UART) are the only 0 bits. Everything else (stop, data and parity bits) including idle time is a 1. Although some extra 0 bits may be generated by the start−up transient, after a short time only valid start bits will remain and the device will be synchronized.

End of Frame

The UART can cause a possible problem at the end of frame. Normally, it is necessary to wait until the last bit of the last character of the frame has been sent until carrier is turned off. The UART usually tells you it's empty which is an indication that you should turn carrier off. However, UARTs differ in when they indicate empty. Some indicate empty at the time of the last shift clock − that is, simultaneously with the stop bit being shifted out. But if carrier were to be turned off at that time, the modem would cease transmitting and the stop bit wouldn't be sent. Therefore, it is important to determine which kind of UART you have. If it behaves as described, then you should wait at least one bit time after the empty indication until you turn off carrier. Note that adding a 1 bit delay can't do any harm, even if it isn't needed.

Misuse of Carrier Detect

To maximize speed, a field instrument will often be designed to begin its response frame immediately after the master's command frame. These frames are close enough together that there is not enough time for carrier detect to drop out. This brings out an important point regarding carrier detect: Its sole purpose is to indicate the presence of carrier so that receivers know that they have sufficient signal to work with. Carrier detect is not intended to reliably indicate the start or end of a particular frame. Start of frame detection is a data link layer function and must occur through examination of the frame content.

Appendix

HART Slave

For detailed information on the HART physical layer specification and requirements, see HCF_SPEC−54.

Note the RC circuit connected to the INRESET pin in Figures 20 and 21. This is a form of POR. Other circuit solutions are possible as long as the reset timing requirements shown in section 3 of the A5191HRT specification are met.

ON Semiconductor recommends using the R and C values depending on the VDD rise and settling times, and application.

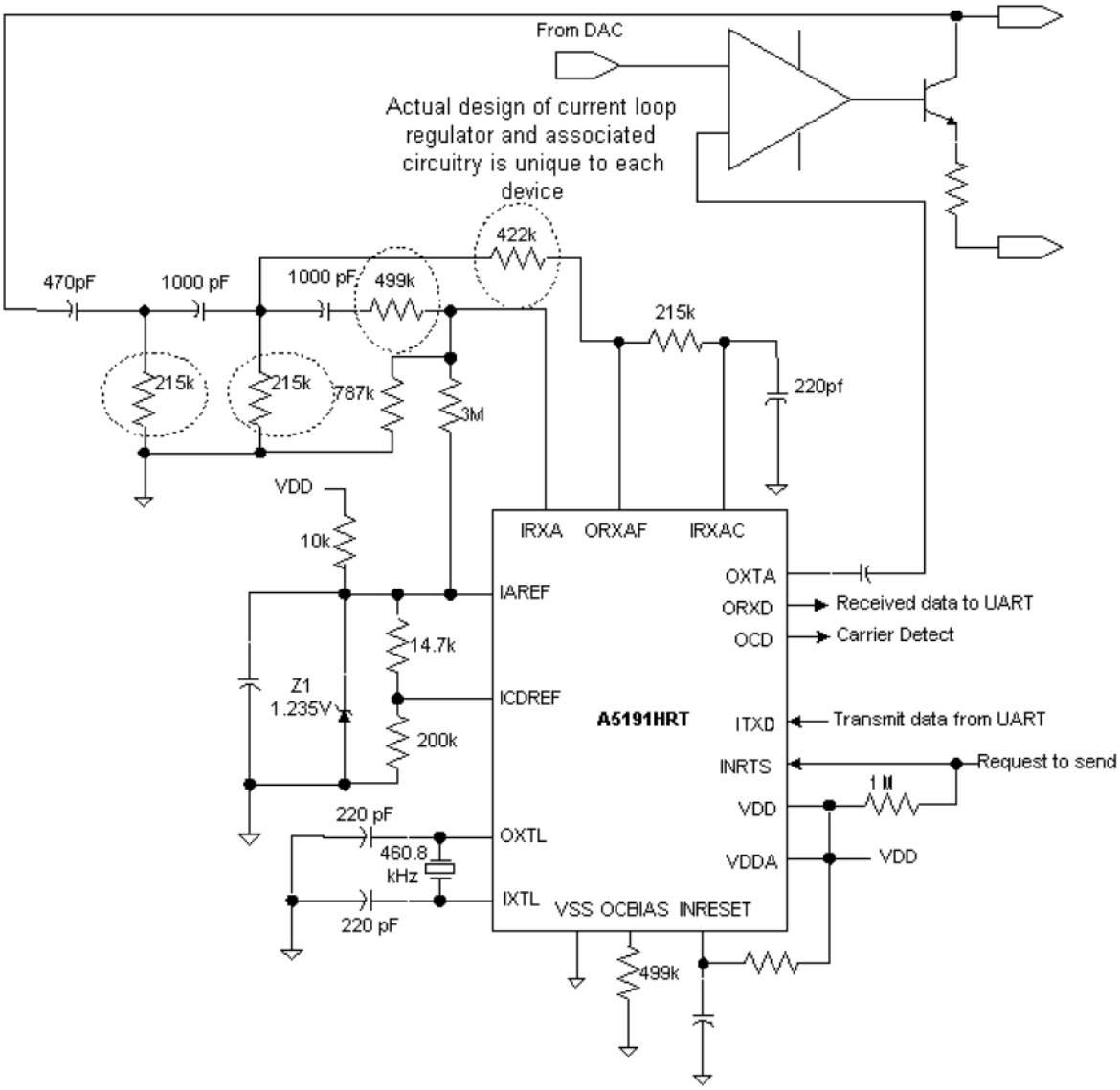

Figure 20. Sample Schematic for HART Slave Physical Layer Circuit Implementation

NOTE: The four resistors circled with a dashed line above in Figure 20 specify different values than those used with the LSI 20C15. In all other respects, the circuit topology and all other component values are identical to the circuit used with the LSI 20C15.

HART Master

HART Primary Master Receiver Requirements

For detailed information on the HART physical layer specification and requirements, see HCF_SPEC−54.

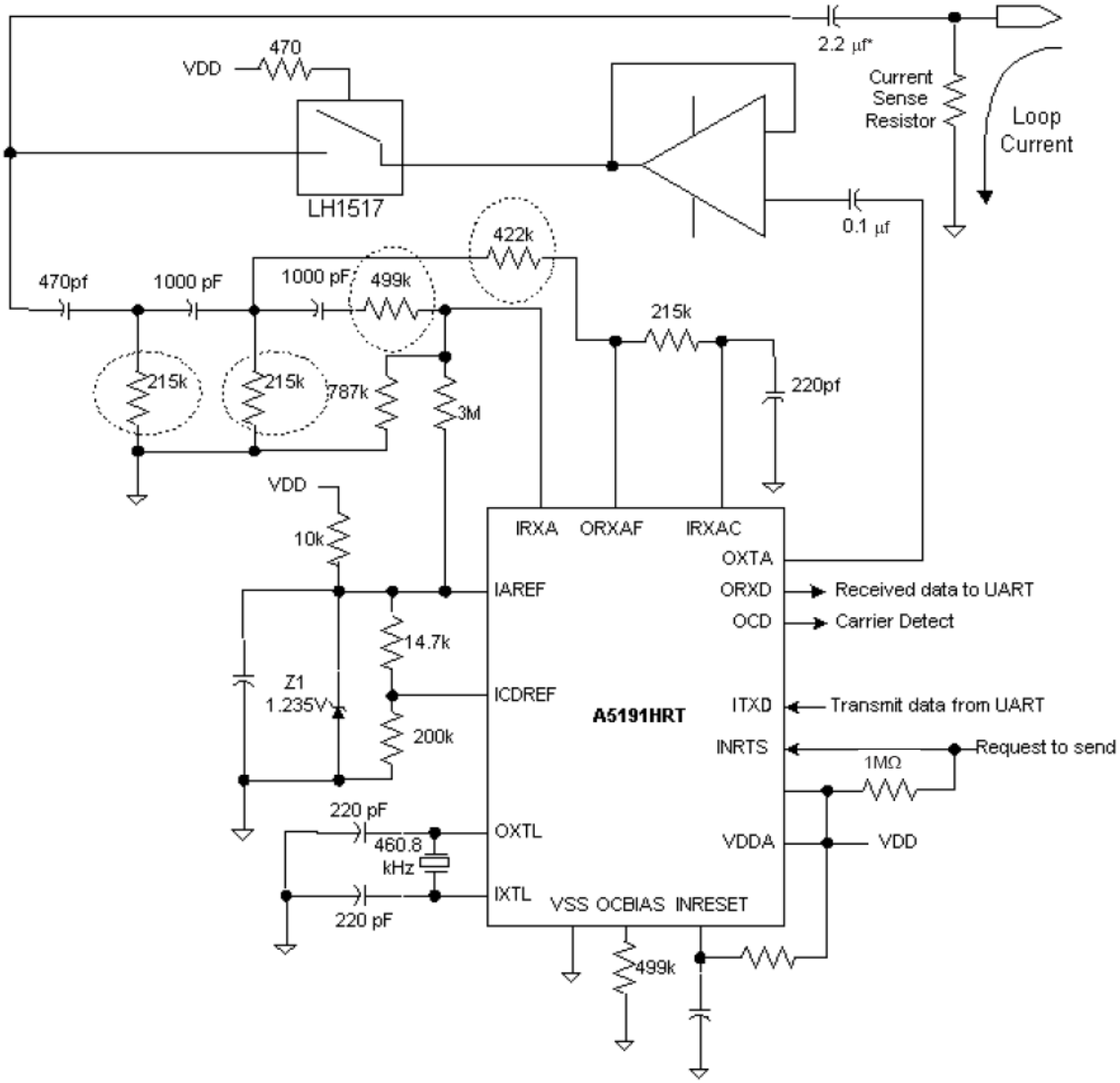

Figure 21. Sample Schematic for HART Master Physical Layer Circuit Implementation

NOTE: The four resistors circled with a dashed line above in Figure 21 specify different values than those used with the LSI 20C15. In all other respects, the circuit topology and all other component values are identical to the circuit used with the LSI 20C15.

A5191HRT Current Consumption

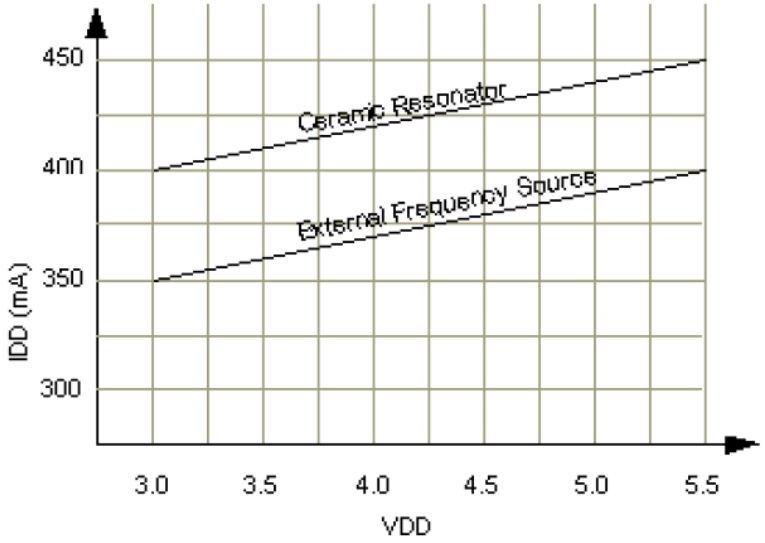

Figure 22. A5191HRT Current Consumption vs. VDD

In Figure 22 the current consumption data is assumes a 499 kΩ bias resistor and that the A5191HRT is receiving and demodulating a message. This is the worst case condition for current consumption.

Table 5. A5191HRT Specification Highlights

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	DC power supply operating voltage		3.3		5.5	VDC
IDD	Total DC operating current	VDD = 3.5 V, ceramic resonator, 500 kΩ bias		400	600	μA
Toper	Operating temperature		−40		85	°C
OTXA	Transmit analog trapezoid waveform	IAREF = 1.235 VDC	400	500	600	mVpp
OXTL/IXTL	Frequency of ceramic resonator or external clock		456.2	460.8	465.4	kHz
IAREF	Analog voltage reference		1.2	1.235	2.6	VDC
ICDREF	Carrier detect reference			IAREF − 0.1		VDC
OCBIAS	Comparator bias current	499 kΩ		2.5		μA

References

1. HART Communication Foundation Document Number HCF_SPEC−54, HART FSK Physical Layer Specification, Revision 8.1; 9390 Research Blvd., Suite I−350, Austin Texas, 78759.
2. HART Communication Foundation Document Number HCF_TEST−2, FSK Physical Layer Test Specification, Revision 2.1 9390 Research Blvd., Suite I−350, Austin Texas, 78759.
3. ON Semiconductor A5191HRT datasheet: http://www.onsemi.com/PowerSolutions/product.do?id=A5191HRT

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